

Thermal Conduction Path Analysis in 3-D ICs

Boris Vaisband¹, Ioannis Savidis², and Eby G. Friedman¹

¹Department of Electrical and Computer Engineering, University of Rochester, Rochester, New York 14627
{bvaisban, friedman}@ece.rochester.edu

²Department of Electrical and Computer Engineering, Drexel University, Philadelphia, Pennsylvania 19104
isavidis@coe.drexel.edu

Abstract—The on-going effort of integrating heterogeneous circuits as well as the increasing length of global interconnect are driving the semiconductor community towards 3-D integrated circuits. In this work, thermal paths within a 3-D stack are investigated using the HotSpot simulator, and the results are compared to experimental data of a fabricated two layer stack with a single back metal layer. Resistive heaters and sensors measure the heat flow in both the horizontal and vertical dimensions. The dependence of the thermal conductivity on temperature is integrated into the thermal simulation process. At high temperatures ($\sim 80^\circ\text{C}$), this effect is responsible for inaccuracies in the temperature and thermal resistance of up to, respectively, 20% and 28%. As confirmed by simulation, those horizontal paths that lie mostly within the silicon layer conduct more heat as compared to the vertical paths, since the thermal conductivity of silicon dioxide is ~ 200 times smaller than the thermal conductivity of silicon.

I. INTRODUCTION

Two important issues in modern ICs are heterogeneity and global signaling. Coupling between different circuits has increased with greater on-chip integration. A natural solution is to use a 3-D structure [1], where each layer is fabricated separately, and all of the layers are stacked to form a heterogeneous system [2]. The 3-D structure also addresses the increasing length of the global interconnects. Much research addresses heat propagation and cooling within 3-D integrated circuits, thermal aware placement and routing, and through silicon via characterization [3]–[8]. As the vertical dimension becomes blocked by additional stacked layers, the heat is not as easily transferred towards the heat sink as in 2-D circuits. An important obstacle is therefore identifying thermal paths within a 3-D stack. Thermal paths within a segment of a 3-D stack, including the thermal through silicon vias, are illustrated in Figure 1. With higher temperature, the mobility of the charge carriers decreases, which consequently slows the circuit. The dependence of the electron mobility on temperature is illustrated in Figure 2 [9], [10].

Thermal flow in materials is described by the Fourier Law,

$$\vec{q} = -k \cdot \nabla T \quad (1)$$

Thermal analysis within a 3-D structure is based on the heat flux density (the energy that flows through a unit area per unit time, or alternatively, the amount of power that flows

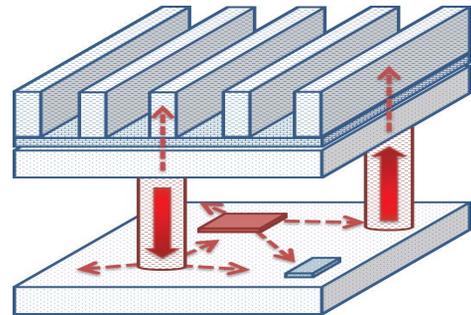


Fig. 1. Heat conduction paths within a 3-D stack.

through a unit of area) \vec{q} [$\frac{W}{m^2}$], the thermal conductivity, a property of the material k [$\frac{W}{m^\circ C}$], and the temperature gradient $-\nabla T$ [$\frac{^\circ C}{m}$]. To avoid a computationally expensive analysis, the three-dimensional form in (1) is reduced to a one-dimensional form, as described by (2). This simplification is sufficiently accurate in 3-D structures, as any thermal path may be broken down into vector components in either the horizontal or vertical dimension. The diagonal paths (in both the horizontal and vertical dimensions) may be superimposed using one-dimensional segments,

$$q_x = k \frac{dT}{dx} \quad (2)$$

Integrating both sides of (2) and assuming that the material in each layer is uniform, the heat transfer equation becomes

$$Q = kA \frac{\Delta T}{\Delta x} \quad (3)$$

Q [W] is the heat transfer rate, and A [m^2] is the surface area through which the heat is transferred. The heat transferred through silicon is depicted in Figure 3. T_1 and T_2 are the temperature measured at, respectively, x_1 and x_2 .

Analogous to electrical interconnect, thermal conduits can be characterized with respect to the thermal resistance (R_{th} [$\frac{^\circ C}{W}$]) [11]. A thermal analogy to Ohm's law is described by

$$R_{th} = \frac{\Delta T}{Q} \iff R = \frac{\Delta V}{I} \quad (4)$$

R_{th} is analogous to the electrical resistance R , ΔT is analogous to the difference in electrical potential $\Delta\phi$, and Q is analogous to the electrical current I . Substituting (3) into (4) yields a linear relationship between the thermal resistance and thermal conductivity, which is also analogous to the

This research is supported in part by the Binational Science Foundation under Grant No. 2012139, the National Science Foundation under Grant No. CCF-1329374, and by grants from Qualcomm, Cisco Systems, and Samsung.

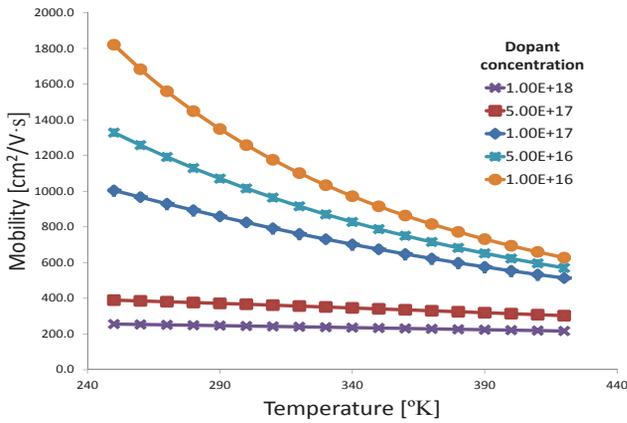


Fig. 2. Electron mobility in silicon as a function of temperature for dopant concentrations ranging from 10^{16} to 10^{18} [cm^{-3}] [9], [10].

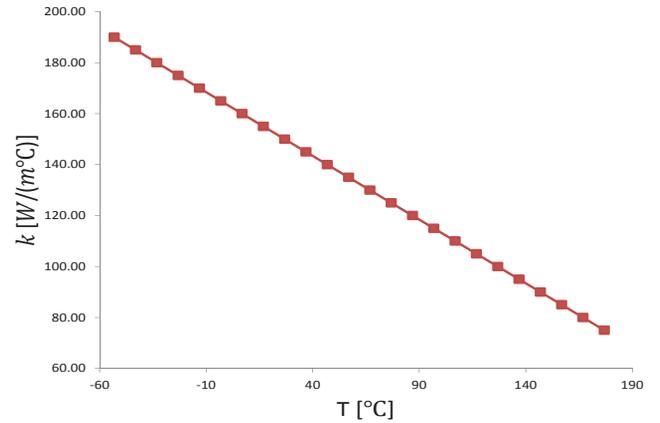


Fig. 4. Thermal conductivity versus temperature for silicon [12]–[14].

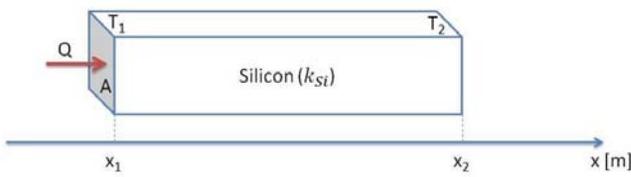


Fig. 3. Heat transfer in silicon.

linear relationship between electrical resistance and electrical conductivity, as shown in (5),

$$R_{th} = \frac{1}{k} \cdot \frac{\Delta x}{A} \iff R = \frac{1}{\sigma} \cdot \frac{L}{A} . \quad (5)$$

The thermal resistance per unit length is an effective metric to analyze the thermal behavior of the horizontal and vertical paths,

$$\frac{R_{th}}{\Delta x} = \frac{1}{k} \cdot A . \quad (6)$$

Both simulations and experimental measurements exhibit the dependence of thermal conductivity on temperature. Previous literature [12]–[16], dating to the early 1960's, shows that within the relevant range of temperatures ($-55^{\circ}C$ to $125^{\circ}C$), k decreases with higher temperatures in materials commonly used in integrated circuits (e.g., silicon, aluminum, and tungsten). An example of the dependence of thermal conductivity on temperature for silicon is illustrated in Figure 4 [12]–[14]. In this example, the thermal conductivity decreases by 47% from $-53.2^{\circ}C$ to $126.9^{\circ}C$.

II. SIMULATION SETUP AND TOOLS

The HotSpot simulator [17], [18] is used in this work to analytically investigate thermal conductivity paths in 3-D structures. To analyze heat propagation within a 3-D stack, including the dependence of thermal conductivity on temperature, the structure shown in Figure 5 is considered. This stack consists of two silicon layers and a single aluminum back metal layer (i.e., the Wtop, Wbottom, and BackMetal layers). The back metal is connected to Wtop using thermal through silicon vias (TTSVs), modeled as a $6 \mu m$ high tungsten via.

Thermally passive (no heat is generated) layers are included in the simulation to better model a practical 3-D structure (e.g., silicon dioxide, bulk silicon, and the metal layers). Two heaters, modeled as heat dissipating blocks, are placed 1.2 mm from each other on each layer. Six heater/sensor sites are placed across the structure to analyze the propagation of heat in both the horizontal and vertical dimensions.

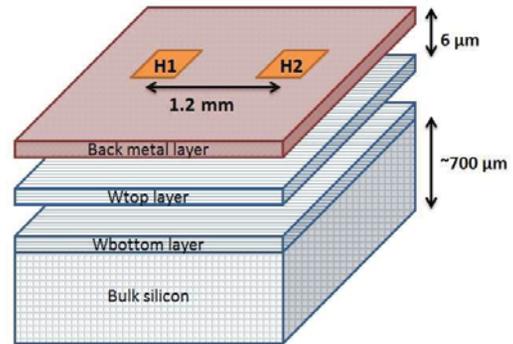


Fig. 5. Structure of a 3-D stack consisting of two silicon layers and one back metal layer. Each layer has two separately controlled heaters (H1 and H2). The back metal is connected to Wtop using thermal through silicon vias.

Different heaters are turned on to model different on-chip power dissipating blocks and related thermal paths. Temperatures are measured at each of the six sites.

The simulations are verified with test data. The stack consists of two layers of silicon with a single back metal layer. Two resistive heater/sensor pairs are placed on each of the silicon layers (on either metal two or three). On the back metal, two resistive structures are used as either a heater or sensor. These structures are relatively large and cannot be stacked since there is only one layer of back metal. Current, ranging from 0 to 110 mA, is passed through the heater structures, and resistances are extracted from the sensor structures. After calibration, these resistance values are converted into temperatures. This setup allows heat propagation paths within the 3-D structure to be experimentally measured and compared to simulation.

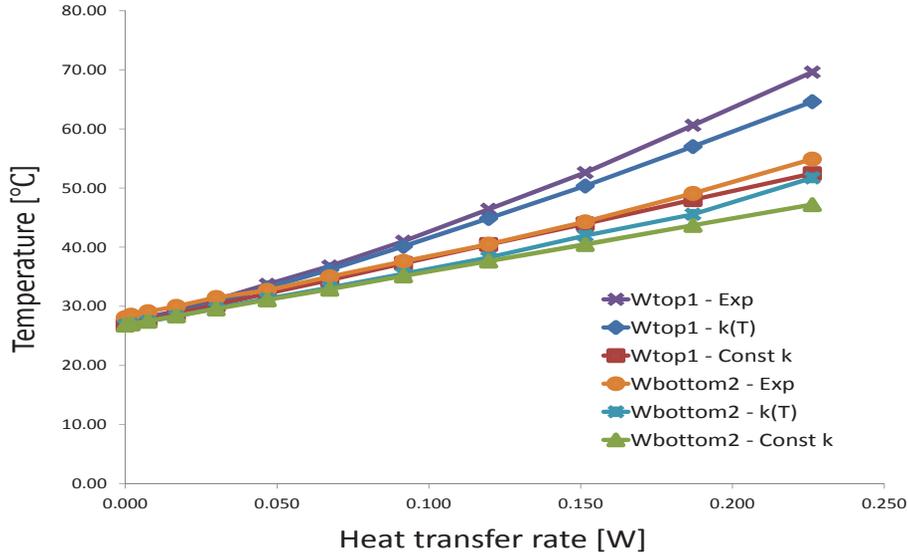


Fig. 6. Temperature measurement for constant thermal conductivity, temperature dependent thermal conductivity, and experimental setup. The Wbottom1 heater is on and temperatures are measured at Wtop1 and Wbottom2.

III. SIMULATION RESULTS

Different thermal paths as well as the dependence of these paths on temperature are evaluated for different levels of power dissipated by the heaters. The measured temperature at two different sensors sites, (i) top layer, first sensor site (Wtop1), and (ii) bottom layer, second sensor site (Wbottom2), are shown in Figure 6. The heater on the bottom layer, first site (Wbottom1), is turned on and dissipates power, analogous to the heat transfer rate Q . The measured temperature for a constant value of k are lower by up to 19% as compared to the measured temperature for the temperature dependent k . A comparison to experimental test data is also provided in Figure 6. The constant k simulations deviate from the experimental results by up to 25%, while for a temperature dependent k , the deviation only reaches 7%. Additional simulation results are listed in Table I.

The thermal resistance per unit length is analytically determined from (4) and (6). The thermal resistance per unit length of two thermal paths: (i) a horizontal path: Wbottom1 heater \rightarrow Wbottom2 sensor, and (ii) a vertical path: Wbottom1 heater \rightarrow Wtop1 sensor, is illustrated, respectively, in Figures 7 and 8. The difference in thermal resistance per unit length between the model based on a constant thermal conductivity and the model based on a temperature dependent thermal conductivity reaches 28%. As compared to experimental results, the constant k results deviate by up to 38%, while the temperature dependent k results deviate by a maximum of 13%. The simulations indicate that the lateral thermal paths conduct more heat as compared to the vertical thermal paths. The thermal resistance per unit length of the vertical path is two orders of magnitude larger than the thermal resistance per unit length of the horizontal path, since SiO_2 exhibits a lower thermal conductivity than silicon.

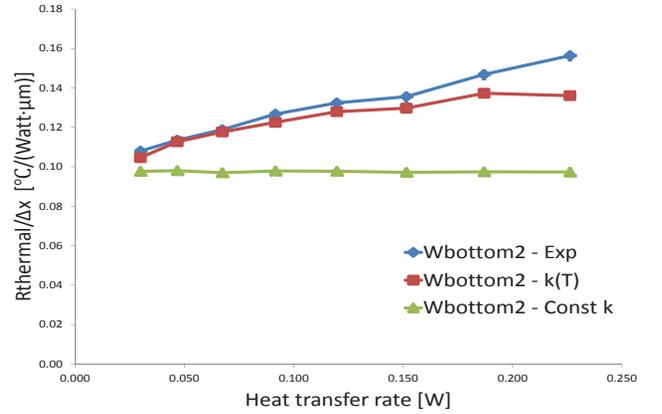


Fig. 7. Thermal resistance for constant thermal conductivity, temperature dependent thermal conductivity, and experimental setup. Horizontal path - Wbottom1 heater is on and temperatures are measured at Wbottom2.

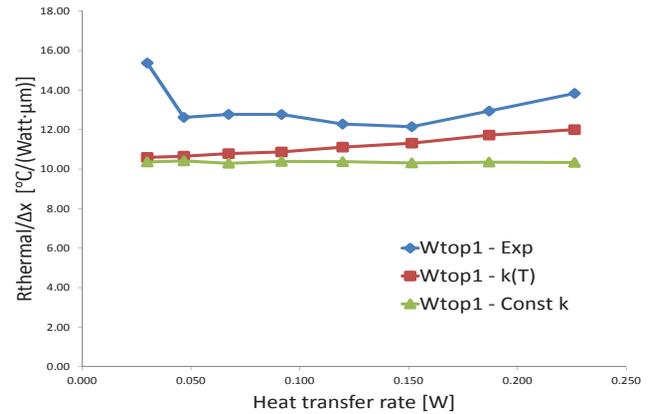


Fig. 8. Thermal resistance for constant thermal conductivity, temperature dependent thermal conductivity, and experimental setup. Vertical path - Wbottom1 heater is on and temperatures are measured at Wtop1.

TABLE I
MEASURED TEMPERATURES AT ALL SENSOR SITES FOR THE CASE WHERE THE WBOTTOM1 HEATER IS ON.

Power generated by heater [W]			0.000	0.002	0.007	0.017	0.030	0.047	0.067	0.092	0.120	0.151	0.187	0.226
Wbottom1 on [°C]	Const k	Wtop1	26.85	27.08	27.64	28.78	30.25	32.17	34.44	37.27	40.44	43.96	48.03	52.45
		Wtop2	26.85	27.03	27.48	28.38	29.55	31.09	32.89	35.15	37.67	40.46	43.71	47.23
		Wbottom1	26.85	27.28	28.37	30.53	33.35	37.04	41.37	46.79	52.86	59.58	67.39	75.84
		Wbottom2	26.85	27.03	27.48	28.38	29.55	31.08	32.88	35.13	37.65	40.44	43.69	47.2
		BackMetal1	26.85	27.03	27.48	28.38	29.55	31.08	32.88	35.13	37.66	40.45	43.69	47.2
		BackMetal2	26.85	27.03	27.48	28.38	29.55	31.08	32.88	35.13	37.65	40.44	43.68	47.19
	k(T)	Wtop1	26.85	27.07	27.67	28.93	30.57	33.14	36.19	40.14	44.86	50.36	57.02	64.6
		Wtop2	26.85	27.02	27.45	28.3	29.67	31.28	33.16	35.51	38.27	41.98	45.58	51.75
		Wbottom1	26.85	27.28	28.39	30.68	33.74	38.12	43.45	50.1	58.16	67.5	78.94	91.75
		Wbottom2	26.85	27.02	27.45	28.3	29.67	31.27	33.15	35.5	38.25	41.95	45.56	51.72
		BackMetal1	26.85	27.02	27.45	28.3	29.67	31.27	33.15	35.51	38.26	41.96	45.57	51.73
		BackMetal2	26.85	27.02	27.45	28.3	29.67	31.27	33.15	35.5	38.25	41.95	45.55	51.71
	Experimental	Wtop1	26.7	27.4	28.2	29.2	31.1	33.7	36.8	41	46.4	52.6	60.6	69.6
		Wtop2	26.9	27.3	27.7	28.5	29.8	31.7	33.3	35.6	38.7	42.4	46.5	52.1
		Wbottom1	27.6	28.4	29.2	31.6	35.7	39.6	45.4	52.7	61.1	71	84.8	100.9
		Wbottom2	28.1	28.5	29.1	30	31.5	32.7	35	37.6	40.5	44.3	49.1	54.9
		BackMetal1	27.3	27.3	27.7	28.7	30.1	31.6	33.9	36.6	40.1	44.4	49.2	55.1
		BackMetal2	27.3	27.3	27.7	28.2	30.1	32	33.9	36.6	40	43.9	49.2	55.6

IV. CONCLUSIONS

In this work, the conduction of heat within a 3-D structure is considered. The horizontal and vertical dimensions are both evaluated for different heat sources. The analysis provides insight into those issues that influence the heat propagation process, such as identification of the thermal paths. The dependence of thermal conductivity on temperatures is also shown to be significant. For certain thermal paths, a constant k produces lower temperatures by up to 19% as compared to a temperature dependent k . In addition, the thermal resistance per unit length of different thermal paths is explored, exhibiting an increase of up to 28% when the temperature dependence of the thermal conductivity is included in the analysis.

The simulation results are compared to experimental test data conducted on a fabricated two layer 3-D stack. Simulations of the constant thermal conductivity deviate by up to 25% for the absolute temperature, and up to 38% for the thermal resistance per unit length, while for a temperature dependent thermal conductivity, the deviations are, respectively, 7% and 13%. In addition, the vertical paths exhibit a larger thermal resistance per unit length as compared to the horizontal paths. This behavior is attributed to the lower thermal conductivity of SiO₂ as compared to silicon. Heat propagation in the vertical dimension is shown to be poor; the heat primarily passes along the horizontal dimension. Vertical heat removal paths are therefore needed to reduce degradations in performance caused by heat accumulation. This analysis confirms the importance of accurately modeling the thermal conductivity, and integrating accurate thermal conductivity models into the thermal analysis process.

REFERENCES

- [1] V. F. Pavlidis and E. G. Friedman, *Three-Dimensional Integrated Circuit Design*, Morgan Kaufmann, 2009.
- [2] S. Bhansali, G. H. Chapman, E. G. Friedman, Y. Ismail, P. R. Mukund, D. Tebbe, and V. Jain, "3-D Heterogeneous Sensor System on a Chip for Defense and Security Applications," *Proceedings of the SPIE Security and Defense Symposium*, pp. 413 – 424, April 2004.
- [3] E. Beyne, "3-D Interconnection and Packaging: Impending Reality or Still a Dream?," *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 138 – 139, February 2004.
- [4] K. Sikka, J. Wakil, H. Toy, and H. Liu, "An Efficient Lid Design for Cooling Stacked Flip-Chip 3-D Packages," *Proceedings of the IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, pp. 606 – 611, June 2012.
- [5] A. Bar-Cohen, "Thermal Management of On-Chip Hot Spots and 3-D Chip Stacks," *Proceedings of the IEEE International Conference on Microwaves, Communications, Antennas and Electronics Systems*, pp. 1 – 8, November 2009.
- [6] M. M. Sabry, A. K. Coskun, D. Atienza, T. S. Rosing, and T. Brunschwiler, "Energy-Efficient Multiobjective Thermal Control for Liquid-Cooled 3-D Stacked Architectures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 30, No. 12, pp. 1883 – 1896, December 2011.
- [7] I. Savidis and E. G. Friedman, "Electrical Characterization and Modeling of 3-D Vias," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 784 – 787, May 2008.
- [8] I. Savidis and E. G. Friedman, "Closed-Form Expressions of 3-D Via Resistance, Inductance, and Capacitance," *IEEE Transactions on Electron Devices*, Vol. 56, No. 9, pp. 1873 – 1881, September 2009.
- [9] S. S. Li and W. R. Thurder, "The Dopant Density and Temperature Dependence of Electron Mobility and Resistivity in N-Type Silicon," *Solid-State Electronics*, Vol. 20, No. 7, pp. 609 – 616, 1977.
- [10] N. D. Arora, J. R. Hauser, and D. J. Roulston, "Electron and Hole Mobilities in Silicon as a Function of Concentration and Temperature," *IEEE Transactions on Electron Devices*, Vol. 29, No. 2, pp. 292 – 295, February 1982.
- [11] W. Huang, *HotSpot - A Chip and Package Compact Thermal Modeling Methodology for VLSI Design*, Ph.D. Thesis, University of Virginia, January 2007.
- [12] C. J. Glassbrenner and Glen A. Slack, "Thermal Conductivity of Silicon and Germanium from 3°K to the Melting Point," *Physical Review*, Vol. 134, No. 4A, pp. 1058 – 1069, May 1964.
- [13] Glen A. Slack, "Thermal Conductivity of Pure and Impure Silicon, Silicon Carbide, and Diamond," *Journal of Applied Physics*, Vol. 35, No. 12, pp. 3460 – 3466, December 1964.
- [14] M. Asheghi, K. Kurabayashi, R. Kasnavi, and K. E. Goodson, "Thermal Conduction in Doped Single-Crystal Silicon Films," *Journal of Applied Physics*, Vol. 91, No. 8, pp. 5079 – 5088, April 2002.
- [15] H. A. Schafft, J. S. Suehle, and P. G. A. Mirel, "Thermal Conductivity Measurements of Thin-Film Silicon Dioxide," *Proceedings of the IEEE International Conference on Microelectronic Test Structures*, pp. 121 – 125, March 1989.
- [16] *Tungsten Sheet Rolling Program Phase I, Technical Progress Report*, Universal - Cyclops Steel Corporation, Bridgeville, Pennsylvania, 1960.
- [17] W. Huang, S. Ghosh, S. Velusamy, K. Sankaranarayanan, K. Skadron, and M. R. Stan, "HotSpot: A Compact Thermal Modeling Methodology for Early-Stage VLSI Design," *IEEE Transactions on Component Packaging and Manufacturing Technology*, Vol. 14, No. 5, pp. 501 – 513, May 2006.
- [18] K. Skadron, M. R. Stan, W. Huang, S. Velusamy, K. Sankaranarayanan, and D. Tarjan, "Temperature-Aware Microarchitecture," *Proceedings of the IEEE International Symposium on Computer Architecture*, pp. 2 – 13, May 2003.