the gate of both bias transistors. The applied voltage to the bias transistors can be modified to modulate the circuit behavior.

III. Simulated Results

An inverter cell is designed and simulated in each logic family. A four-inverter chain is used to evaluate the total power, area, performance, and noise margins. Prior work on near-threshold computing has not considered the robustness of the circuit to noise. The nominal supply voltage is set to 1.2 V for all logic families. The supply voltage is set to 400 mV when operating at near-threshold.

A. Characterization of power, area, and performance among different logic families

The performance in terms of maximum operating frequency, area, and power consumption of the different logic families are listed in Table I, where DCML outperforms all other logic families. From the listed results, DCML operates at the highest frequency and consumes the least power from all logic families. Each logic family is designed for minimum area and full swing at the end of the fourth stage when operating at a near-threshold voltage. Among all logic families, DCML is the fastest and CMOS the slowest. The maximum operating frequency of the CMOS inverter chain is 63 MHz. Therefore, to fairly compare the logic families, the operating frequency is set to 60 MHz and the area, power, and robustness to noise is analyzed. At a 60 MHz operating frequency and 400 mV supply voltage, the DCML inverter chain consumes 32% less power than the CMOS inverter chain. Using a DCML inverter chain at a near-threshold voltage reduces the total power consumption by 93% but incurs a 33x penalty in performance as compared to a CMOS inverter chain operating at a nominal supply voltage of 1.2 V and with the same area constraint. In addition, the total power consumption is reduced by 92% with a 64% improvement in performance when using DCML over CML at a near-threshold supply voltage.

For applications with strict static power requirements, SDCML provides the best solution. At near-threshold voltages, the CMOS inverter consumes 9.64x times the static power as compared to an SDCML inverter. In contrast, the "always on" tail transistor of the CML inverters increases the overall static power consumption. Therefore, at near-threshold voltages, the CML inverters consume 81250x (4550 nW) times the static power as compared to SDCML inverters, as listed in Table I. In addition, the static power consumption of the SDCML inverter is reduced to 0.01% of the total power consumption at a near-threshold voltage.

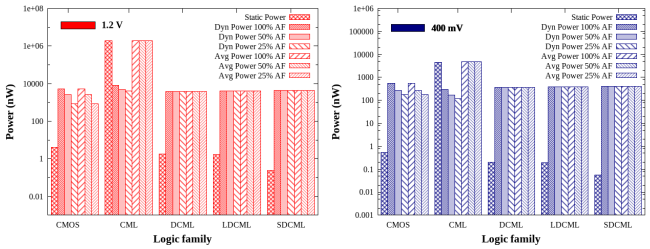
TABLE I: Performance, area, and power comparison at a 400 mV supply voltage.

	CMOS	CML	DCML	LDCML	SDCML
Max freq. with 4 stages (*MHz*)	63	70	115	100	90
Area (μm^2)	2.88	10.56	4.56	4.85	5.9
Static power (*nW*)	0.54	4550	0.2	0.19	0.056
Dynamic power (*nW*)	544.46	300	368.8	393.81	409.94
Total power (*nW*)	545	4850	369	394	410

B. Characterization of total power consumption for different activity factors (AF)

Dynamic power consumption is reduced with lower activity factor for CMOS logic. However, for DCML, the dynamic power does not change with activity factor. DCML circuits are therefore beneficial to reduce noise on the power delivery network. CML also exhibits minor changes in power consumption with a change in activity factor. The power consumption for different activity factors is shown in Fig. 4. The nominal 1.2 V and near-threshold 400 mV supply voltages are shown in Fig. 4(a) and 4(b), respectively. For all logic families and supply voltages, the operating frequency of the inverter chain is set to 60 MHz.

Among all logic families, SDCML consumes the least static power both at a nominal and near-threshold voltage. The majority of the total power consumed by CML is static for all supply voltages. The majority of the total power consumption of DCML logic families, however, is dynamic. The average power shown in Fig. 4, represents the total power consumed per cycle for different activity factors. The maximum power savings is achieved at higher activity factors. An input signal with a period of 8.33 ns is used to produce a 60 MHz operating frequency at near-threshold voltages. The maximum allowed propagation delay is set to 5.831 ns (70% of the signal period) for the DCML logic families.



(a) (b)

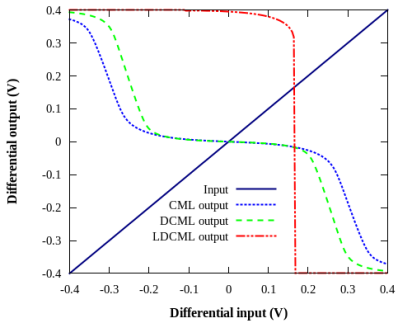
Fig. 4: Power consumption of the logic families for different activity factors when the supply voltage is set to a) 1.2 V, and b) 400 mV.

C. Noise analysis

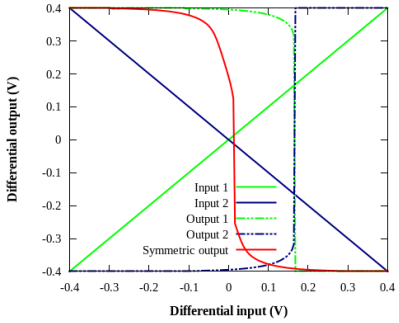
An analysis of the noise margins is done at both the nominal and near-threshold supply voltages at a set frequency of 60 MHz to characterize the robustness of the logic families. A conventional voltage transfer curve (VTC) is used to determine the noise margin of the CMOS inverter [8]. However, CML and DCML inverters are evaluated by differential inputs. As the inverter ***Input*** and ***Output*** are both differential signals, the VTC curve represents the difference in the two input and two output signals, as shown in Fig. 5 (a).

A comparison of the noise margins for all logic families at both a nominal and near-threshold voltage is shown in Fig. 6. The noise margin high (NM_H) is always a positive voltage, and the noise margin low (NM_L) is always negative for the proposed inverter circuits. However, to simplify the comparison and analysis of the logic families, the absolute value of the NM_L is used to calculate the values shown in Fig. 6 for all DCML inverters. Both at a nominal and near-threshold voltage, the noise margin of the LDCML inverter is greater than all other logic families. At near-threshold, the NM_H and NM_L of an LDCML inverter are, respectively, 228 mV and 564 mV for a differential input starting at 400 mV and finishing at -400 mV. In comparison, the NM_H and NM_L of a CMOS inverter are, respectively, 161 mV and 90 mV.

For LDCML, one of the differential input paths dominates the other based on the initial input voltages on the inverter (due to the PMOS latches). Therefore, the initial zero voltage on the N1 transistor results in a differential NM_L of 564 mV, which is higher than the voltage applied to any single input. An analysis of differential inputs starting with the opposite



(a)



(b)

Fig. 5: Simulated VTC of a) all differential inverters at a 400 mV supply voltage, and b) an LDCML inverter at a 400 mV supply voltage for the two directional input polarity sweeps and two NMOS transistor sizes.

polarity (differential input of -400 mV) result in a NM_H of 564 mV and NM_L of 228 mV. The voltage transfer curve (VTC) of an LDCML inverter with opposite input polarities is shown in Fig. 5 (b) and the corresponding noise margins are shown in Fig. 6 (marked as inverted input). In Fig. 5 (b), Input 1 represents the differential input with values for In and $\overline{In}$ initially set to, respectively, 400 mV and 0 V. Input 2 represents the opposite differential input condition where the values of In and $\overline{In}$ are initially set to, respectively, 0 V and 400 mV. The asymmetric behavior of the VTC is corrected by increasing the size of the NMOS transistors by 20 fold, resulting in a symmetric output, as shown in Fig. 5 (b). The large NMOS transistors sink current from the output node with a moderate gate voltage, even as the holding PMOS latch is supplying additional charge. As a result, the NM_L and NM_H are equal regardless of the input polarities. In addition, the asymmetric behavior applies only when the differential input approaches zero, which is not a permitted operating point for the circuit. Therefore, the asymmetric behavior of the noise margins for the LDCML does not effect the circuit operation, while providing additional power savings and speedup as compared to the symmetric implementation. Depending on the applications and specific circuit biasing requirements, the differential inputs are set to either enhance the NM_L or NM_H of the LDCML inverter.

IV. Conclusions

Three DCML inverters are proposed for near-threshold computing that provide improved power, performance, and robustness to noise as compared to CMOS and CML inverters. The proposed DCML inverter operating at a near-threshold voltage

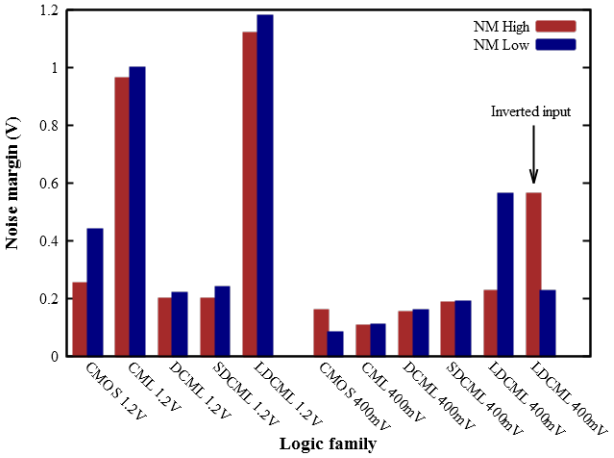


Fig. 6: Comparison of the noise margins of the logic families.

reduces the total power consumption by 92% as compared to a CML inverter while also improving performance by 64%. In addition, the total power consumption of the DCML inverter chain is reduced by 32% as compared to a CMOS inverter chain at near-threshold. At near-threshold, the maximum operating frequency of the DCML inverter chain is 1.83x times greater than CMOS. The LDCML inverter provides the largest noise margins at near-threshold operation among all logic families, with a 1.4x larger high (or low) and 6.7x larger low (or high) noise margin as compared to a CMOS inverter. The SDCML reduces static power by 88% as compared to a CMOS inverter operating at near-threshold.

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