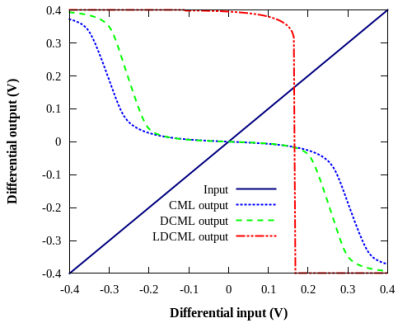
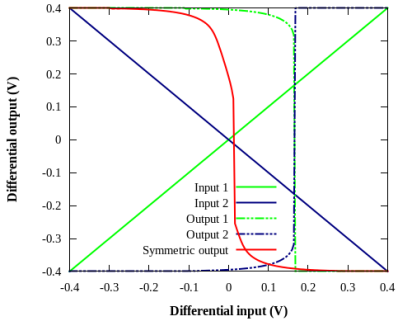


(a)



(b)

Fig. 5: Simulated VTC of a) all differential inverters at a 400 mV supply voltage, and b) an LDCML inverter at a 400 mV supply voltage for the two directional input polarity sweeps and two NMOS transistor sizes.

polarity (differential input of -400 mV) result in a NM_H of 564 mV and NM_L of 228 mV. The voltage transfer curve (VTC) of an LDCML inverter with opposite input polarities is shown in Fig. 5 (b) and the corresponding noise margins are shown in Fig. 6 (marked as inverted input). In Fig. 5 (b), Input 1 represents the differential input with values for In and $\overline{In}$ initially set to, respectively, 400 mV and 0 V. Input 2 represents the opposite differential input condition where the values of In and $\overline{In}$ are initially set to, respectively, 0 V and 400 mV. The asymmetric behavior of the VTC is corrected by increasing the size of the NMOS transistors by 20 fold, resulting in a symmetric output, as shown in Fig. 5 (b). The large NMOS transistors sink current from the output node with a moderate gate voltage, even as the holding PMOS latch is supplying additional charge. As a result, the NM_L and NM_H are equal regardless of the input polarities. In addition, the asymmetric behavior applies only when the differential input approaches zero, which is not a permitted operating point for the circuit. Therefore, the asymmetric behavior of the noise margins for the LDCML does not effect the circuit operation, while providing additional power savings and speedup as compared to the symmetric implementation. Depending on the applications and specific circuit biasing requirements, the differential inputs are set to either enhance the NM_L or NM_H of the LDCML inverter.

IV. Conclusions

Three DCML inverters are proposed for near-threshold computing that provide improved power, performance, and robustness to noise as compared to CMOS and CML inverters. The proposed DCML inverter operating at a near-threshold voltage

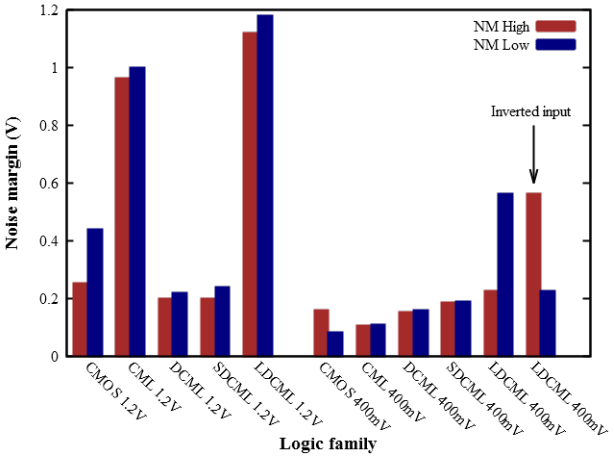


Fig. 6: Comparison of the noise margins of the logic families.

reduces the total power consumption by 92% as compared to a CML inverter while also improving performance by 64%. In addition, the total power consumption of the DCML inverter chain is reduced by 32% as compared to a CMOS inverter chain at near-threshold. At near-threshold, the maximum operating frequency of the DCML inverter chain is 1.83x times greater than CMOS. The LDCML inverter provides the largest noise margins at near-threshold operation among all logic families, with a 1.4x larger high (or low) and 6.7x larger low (or high) noise margin as compared to a CMOS inverter. The SDCML reduces static power by 88% as compared to a CMOS inverter operating at near-threshold.

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