[6]. Specialized techniques are therefore required to ensure that each device plane is operational, while not exceeding a target output impedance [7]. The *IR* voltage drops and *L·di/dt* switching noise are affected by the density and electrical characteristics of the TSVs [8]. A comparison of two different via densities for identical power distribution networks is presented, and the effects of the 3-D via density on the power network design process are discussed.

The fabricated test circuit is 2 mm × 2 mm, and composed of four equal area quadrants (see Fig. 1b). Three quadrants are used to evaluate the effects of the power distribution network topology on the noise propagation characteristics, and one quadrant is dedicated to DC-to-DC conversion. Each stacked power network is 530 µm x 500 µm, and includes three discrete two-dimensional power networks, one network on each of the three device planes. The total area occupied by each block is less than 0.3 mm^2, representing a portion of a power delivery network. Each block includes the same logic circuit but utilizes a different power distribution architecture. The power supply voltage is 1.5 volts for all of the blocks. The third MITLL 3-D multi-project wafer includes 1.25 µm diameter TSVs, and CMOS devices with channel lengths of 150 nm. The different power distribution topologies are reviewed in Section III-A, and experimental results are provided in Section III-B.

A. 3-D power topologies

Three topologies to distribute power within a 3-D circuit have been designed and manufactured, and an analysis of the peak noise voltage, voltage range, and average noise for the power and ground network is described. Interdigitated power/ground lines are used in all of the topologies. The four main objectives for the test circuit are to i) determine the peak and average noise within the power and ground distribution networks, ii) determine the effects of the board level decoupling capacitors on reducing undesired noise, iii) explore the effects of a dedicated power/ground plane on the power noise, and iv) investigate the effects of the TSV density on the noise characteristics of the power network. The three power network topologies are illustrated in Fig. 3. The difference between the left (Block 1) and central (Block 2) topologies is the number of TSVs, where the latter topology contains 50% more TSVs. The third topology (Block 3) replaces the interdigitated power and ground lines on the second device plane with two metal planes to evaluate the benefit of dedicated power and ground planes on delivering current within a 3-D system.

B. Experimental results

The peak noise for each topology, with or without a board level decoupling capacitance, is shown in Fig. 4. No single topology contributes the largest noise voltage at any specific bias voltage. The average noise for each topology is approximately 75% to 90% lower than the peak-to-peak voltage, indicating that a majority of the data is located within close proximity of the nominal power and ground voltages.

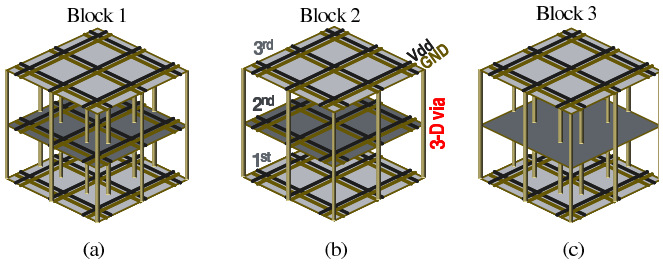

Fig. 3. Power distribution network topologies. (a) interdigitated power network on all planes with the 3-D vias distributing current on the periphery and through the middle of the circuit, (b) interdigitated power network on all planes with the 3-D vias distributing current on the periphery, and (c) interdigitated power network on planes 1 and 3 and power/ground planes on plane 2 with the 3-D vias distributing current on the periphery and through the middle of the circuit.

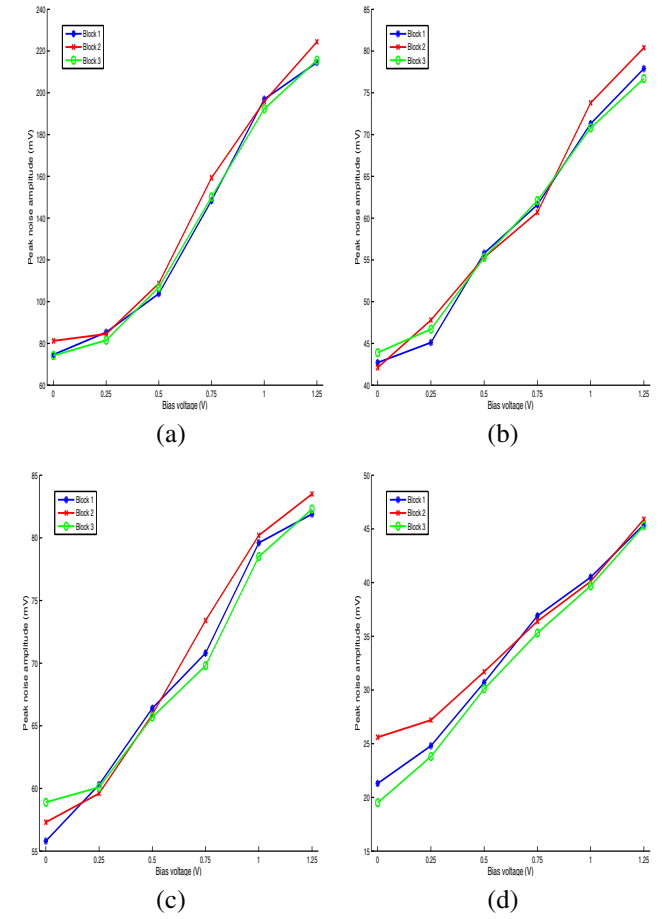

Fig. 4. Peak noise voltage on the power and ground distribution networks with and without board level decoupling capacitance. (a) peak noise of power network without decoupling capacitance, (b) peak noise of power network with decoupling capacitance, (c) peak noise of ground network without decoupling capacitance, and (d) peak noise of ground network with decoupling capacitance.

In addition, the saturation voltage of the detection circuitry at the output node (port0) is approximately 230 mV when the gain is -4.2 dB. The noise detection range is approximately 600 mV centered around 1.5 volts and 0 volts, respectively, for the power and ground lines. The detection circuits for the power network, therefore, detect noise that ranges from 1.2 volts to 1.8 volts, and for the ground networks from -0.3 volts to 0.3 volts.

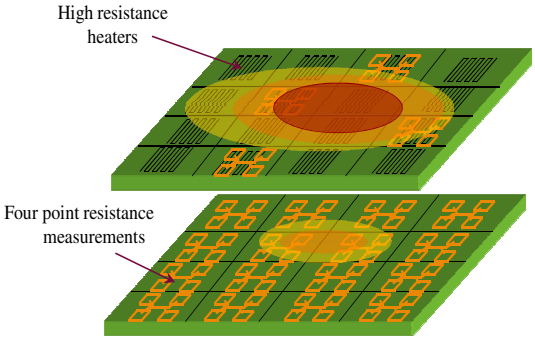

Fig. 5. Test structure to evaluate cross-plane thermal coupling including resistive thermal sources and four-point resistance measurement based thermal sensors.

IV. Thermal Coupling in 3-D Integrated Systems

The third test circuit has been fabricated by Tezzaron Semiconductor in a 130 nm CMOS technology with 1.2 µm diameter TSVs. The test structures have been developed to evaluate thermal coupling between adjacent planes and decoupling capacitor placement within a 3-D system. This test circuit was designed to better understand the effect of inter- and intra-plane thermal resistances on hot spot formation. The test structures that investigate thermal coupling between adjacent planes include both thermal sources and thermal sensors, as shown in Fig. 5. Each thermal source is paired with a thermal sensor on an adjacent metal level, and these pairs are distributed throughout each plane within a 3-D stack. The thermal sources are heater resistors with a target resistance of 8 ohms and a maximum applied voltage of 40 volts. The temperature sensor provides a calibrated four-point measurement tested with a low current to avoid joule heating.

The test circuit on decoupling capacitor placement evaluates the effect of board level decoupling capacitors on *IR* and *L·di/dt* noise in 3-D circuits. A schematic diagram of the four topologies used to analyze decoupling capacitor placement is depicted in Fig. 6. The first two topologies do not include an on-chip decoupling capacitor. The structure pictured in Fig. 6(b) includes a board level capacitor. Test structures with on-chip capacitors are shown in Figs. 6(c) and 6(d). The larger capacitors shared between the two planes are depicted in Fig. 6(c), and a more standard 2-D approach to decoupling capacitor placement where localized point-of-load capacitors are distributed within each plane is shown in Fig. 6(d).

V. Conclusions

Three test circuits examining the critical physical design issues in 3-D systems are reviewed in this paper. Test data examining clock and power distribution networks in 3-D integrated circuits indicate that the choice of 3-D topology greatly affects the skew and noise propagation characteristics, respectively, of clock and power networks. The third test circuit on intra- and inter-plane thermal coupling is currently being fabricated, and is expected to produce insight into thermal management methodologies and decoupling capacitor relocation algorithms.

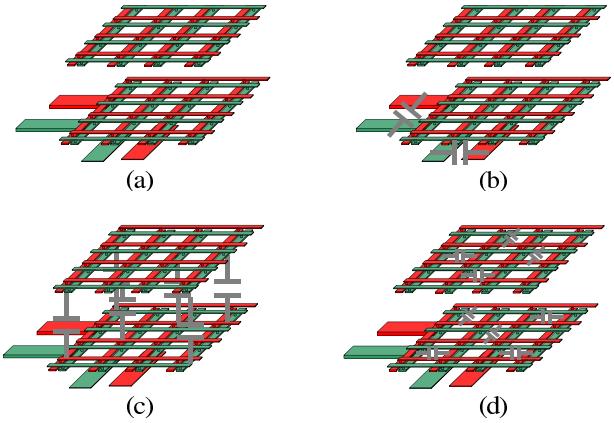

Fig. 6. Schematic diagram of test circuit examining decoupling capacitor placement for a) no decoupling capacitors, b) board level decoupling capacitors, c) inter-plane shared capacitors, and d) point-of-load decoupling capacitors.

3-D integration requires clock and power topologies that are infeasible in 2-D circuits. The ability of 3-D integrated circuits to dedicate multiple planes to the clock or power network supports the development of novel clock and power topologies, permitting die area and metal resources to be strategically allocated. As demonstrated by the experimental data described in this paper, a topology incorporating power and ground planes reduces the maximum noise voltage within a power network by 2% to 18% as compared to more standard interdigitated structures. The experimental data also verify that the block with an H-tree topology on all three device planes produces the lowest skew between planes at the expense of increased power consumption. The topology with H-trees on all three planes operates at 1.4 GHz, the highest frequency of the three clock topologies.

The interdependencies among synchronization, power delivery, and thermal management in 3-D systems demand greater attention. These test circuits provide experimental insight to enhance the development of next generation 3-D integrated circuits.

References

[1] E. G. Friedman (Ed.), *Clock Distribution Networks in VLSI Circuits and Systems*, IEEE Press, 1995.

[2] E. G. Friedman, "Clock Distribution Networks in Synchronous Digital Integrated Circuits," *Proceedings of the IEEE*, Vol. 89, No. 5, pp. 665–692, May 2001.

[3] MIT Lincoln Laboratories, Cambridge, *MITLL Low-Power FDSOI CMOS Process Design Guide*, 2006.

[4] V. F. Pavlidis, I. Savidis, and E. G. Friedman, "Clock Distribution Networks in 3-D Integrated Systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 19, No. 12, pp. 2256–2266, December 2011.

[5] G. Huang, M. Bakir, A. Naeemi, H. Chen, and J. D. Meindl, "Power Delivery for 3D Chip Stacks: Physical Modeling and Design Implication," *Proceedings of the IEEE Electrical Performance of Electronic Packaging*, pp. 205–208, October 2007.

[6] V. F. Pavlidis and E. G. Friedman, *Three-Dimensional Integrated Circuit Design*, Morgan Kaufmann, 2009.

[7] R. Jakushokas, M. Popovich, A. V. Mezhiba, S. Kose, and E. G. Friedman, *Power Distribution Networks with On-Chip Decoupling Capacitors, Second Edition*, Springer, 2011.

[8] I. Savidis and E. G. Friedman, "Closed-Form Expressions of 3-D Via Resistance, Inductance, and Capacitance," *IEEE Transactions on Electron Devices*, Vol. 56, No. 9, pp. 1873–1881, September 2009.