Biographical Sketch

Ioannis Savidis
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A. Professional Preparation

College/University	Location	Major	Degree & Year
Duke University	Durham, NC	Biomedical Engineering Electrical and Computer Engineering	B.S.E., 2005
University of Rochester	Rochester, NY	Electrical and Computer Engineering	M.S., 2007
University of Rochester	Rochester, NY	Electrical and Computer Engineering	Ph.D., 2013

B. Academic/Professional Appointments

2013-present	Assistant Professor, Electrical and Computer Engineering, Drexel University, Philadelphia, Pennsylvania
2006-2013	Graduate Research Assistant, Electrical and Computer Engineering, University of Rochester, Rochester, New York
2009-2011	Independent Contractor, System on Package and 3-D Integration Group, IBM Corporation, Yorktown Heights, New York
Summers 2008, 2009	Research Intern, System on Package and 3-D Integration Group, IBM T. J. Watson Research Center, Yorktown Heights, New York
Summer 2007	Research Intern, Advanced Interconnect and 3-D Integration Group, Freescale Semiconductor, Austin, Texas

C. Products

Products Most Closely Related to Proposal

1. K. Juretus and I. Savidis, "Reducing Logic Encryption Overhead Through Gate Level Key Insertion," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1714-1717, May 2016.
2. K. Juretus and I. Savidis, "Reduced Overhead Gate Level Logic Encryption," *Proceedings of the IEEE/ACM Great Lakes Symposium on Very Large Scale Integration (GLSVLSI)*, pp. 15-20, May 2016.
3. D. Pathak, M. H. Hajkazemi, M. K. Tavana, H. Homayoun, and I. Savidis, "Energy Efficient On-Chip Power Delivery with Run-Time Voltage Regulator Clustering," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1210-1213, May 2016.
4. M. K. Tavana, D. Pathak, M. H. Hajkazemi, M. Malik, I. Savidis, and H. Homayoun, "Realizing Complexity-Effective On-Chip Power Delivery for Many-Core Platforms by Exploiting Optimized Mapping," *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, pp. 618-625, October 2015.
5. I. Savidis, S. Kose, and E. G. Friedman, "Power Noise in TSV-Based 3-D Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 48, No. 2, pp. 587-597, February 2013.

Other Significant Products

1. D. Pathak and I. Savidis, "Run-Time Voltage Detection Circuit for 3-D IC Power Delivery," *Proceedings of the IEEE International System-on-Chip Conference (SOCC)*, pp. 244-249, September 2014.
2. M. K. Tavana, M. H. Hajkazemi, D. Pathak, I. Savidis, and H. Homayoun, "ElasticCore: Enabling Dynamic Heterogeneity With Joint Core and Voltage/Frequency Scaling," *Proceedings of the IEEE/ACM Design Automation Conference (DAC)*, pp. 1-6, June 2015.
3. J. Xue, A. Garg, B. Ciftcioglu, J. Hu, S. Wang, I. Savidis, M. Jain, R. Berman, P. Liu, M. Huang, H. Wu, E. Friedman, G. Wicks, and D. Moore, "An Intra-Chip Free-Space Optical Interconnect," *Proceedings of the 37th Annual International Symposium on Computer Architecture (ISCA)*, pp. 94-105, June 2010.
4. I. Savidis and E. G. Friedman, "Physical Design Trends for Interconnects," *On-Chip Communication Architectures System on Chip Interconnect*, S. Pasricha and N. Dutt, Morgan Kaufmann Publishers, Elsevier, Chapter 11, pp. 403-437, 2008.
5. V. Pavlidis, I. Savidis, and E. G. Friedman, "Clock Distribution Networks in 3-D Integrated Systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 19, No. 12, pp. 2256-2266, December 2011.

D. Synergistic Activities

- **Associate Editor:** *IEEE Transactions on Very Large Scale Integration (VLSI) Circuits*, 2013-present; *Microelectronics Journal*, 2013-present; *Journal of Circuits, Systems, and Computers*, 2013-present
- **IEEE Student Branch Faculty Advisor**, Drexel University, 2014-present; participate in community outreach programs to middle and high school students; provide guidance and support to undergraduate student IEEE members; help plan multi-university undergraduate and graduate student events including this years (January 2015) inaugural Dragon Hacks (first Major League Hacking sanctioned event at Drexel University)
- **Technical Program Committee Member**, IEEE Great Lakes Symposium on Very Large Scale Integration (GLSVLSI), 2013-2015; IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), 2010
- **Technical Reviewer:** *IEEE Transactions on Very Large Scale Integration (VLSI) Circuits* (TVLSI); *IEEE Transactions on Electron Devices* (TED); *IEEE Transactions on Circuits and Systems-II* (TCAS-II); *IEEE Transactions on Computer-Aided Design* (TCAD); *IEEE Transactions on Electron Device Letters* (TEDL); *ASP Journal of Low Power Electronics* (JOLPE); *Analog Integrated Circuits and Signal Processing* (ALOG); *Microelectronics Journal*, *IEEE Transactions on Advanced Packaging* (TADVP); *IEEE Transactions on Components*

E. Collaborators and Other Affiliations

1. Collaborators (17): Syed M. Alam (Everspin Technologies Inc.), Berkehan Ciftcioglu (Intel Corporation), Mark Hempstead (Tufts University), Houman Homayoun (George Mason University), Michael Huang (University of Rochester), Ankur Jain (University of Texas at Arlington), Renatas Jakushokas (Qualcomm Corporation), John U. Knickerbocker (IBM), Selcuk Kose (University of South Florida), Duncan Moore (University of Rochester), Bahram Nabet (Drexel University), Vasilios Pavlidis (University of Manchester), Emre Salman (State University of New York at Stony Brook), Baris Taskin (Drexel University), Gary Wicks (University of Rochester), Hui Wu (University of Rochester), Jing Xue (Qualcomm Corporation)

2. Doctoral advisor (1): Eby G. Friedman (University of Rochester)

3. Current students (5): Isuru Daulagala (M.S. student), Shazzad Hossain (Ph.D. student), Kyle Juretus (Ph.D. student), Divya Pathak (Ph.D. candidate), Vaibhav Venugopal Rao (M.S. student)