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SRC, SIA Tackle Ultra-Low Power SoC Design Challenges for 'Extremely Scaled' Silicon via University Competition Results

Harvard, Virginia, Michigan State Top Two-Year Duel of National Universities

SRC Student Symposium 2006

RESEARCH TRIANGLE PARK, N.C.--(BUSINESS WIRE)--Semiconductor Research Corporation (SRC), the world's leading university-research consortium for semiconductors and related technologies, today announced that a team of graduate students from Harvard University won first place in the SRC/SIA SoC Design Challenge. Culminating a two-year competition that pitted 39 of the best university semiconductor engineering programs in the country, the \$25,000 prize was presented to Professor Gu-Yeon Wei, who led the Harvard team.

"Experience is the best teacher," said Wei of the rigorous challenges of the competition. "It's been getting more difficult for students to have the opportunity to turn their ideas into reality. The SRC/SIA challenge was an invaluable experience for this new generation of chip designers, teaching them about the harsh realities of the increasing complexities facing the IC industry."

Cash awards totaling \$50,000 were presented today at the SRC Student Symposium 2006, where 150 graduate students described their research to companies representing the semiconductor industry. The top five contest teams had an opportunity to see their creative work translated into actual silicon devices using a 180-nanometer CMOS technology fabricated through MOSIS. Teams from the University of Virginia and Michigan State University took second and third places in the final competition.

"Without new concepts and fresh passion from the incoming generation of engineers and scientists, the expectations for future generations of semiconductors are at risk," said Larry Sumney, CEO and president of SRC. "The realities and creativity featured in these competitions help calibrate the universities and businesses as to where design strengths and challenges exist. SRC is pleased to have completed this third university contest, each focusing on a key aspect of leading-edge semiconductor chip design. These contests give member companies access to a broad range of faculty and students on a national level and are one way the chip industry helps ensure a continuing supply of talented design engineers."

The Harvard entry, "Design and Implementation of an Ultra-Low-Power, Event-Driven System Architecture for Sensor Network Applications," targets extreme energy efficiency for use in remote sensor applications. The design could have wide applications in sensors used for homeland security, environmental protection, and monitoring building structures. Beneficiaries of this research include chipmakers and end-users worldwide for communications, computing, aeronautics and aerospace applications, medical devices, automotive and consumer electronics, and a wide range of other applications.

The press for low-power-consuming integrated systems-on-a-chip is largely driven by the growth of

portable applications. However, the design of complex low-power chips encompassing several types of signals is challenging, and is exacerbated by the increased off-state leakage in scaled transistors and by increased power dissipation in interconnect systems. Innovations in circuit design methodologies are seen as vital to overcoming increasing technology limitations.

"Attracting the best and the brightest to pursue careers in science and engineering is one of the greatest challenges to maintaining U.S. leadership in technology," said SIA President George Scalise. "The system-on-a-chip design contest has proved to be a very effective way to dramatize how creativity and innovation in microelectronics contribute to the advancement of virtually every aspect of human endeavor."

The purpose of the SoC Design Challenge is to encourage university faculty and their graduate students to create novel, low-power, robust System-on-Chip (SoC) designs demonstrating the value of greater systems integration in IC design. The contest was also intended to promote education in design of SoC-integrated circuits.

SoC circuits of this complexity have millions of transistors and present many opportunities for human error during design and layout. Engineering students learning design of integrated circuits rarely get the opportunity to take a design through all the steps of circuit fabrication in an advanced technology because of the high cost involved. The creativity of the student teams to design complex and innovative integrated circuits operating in mixed signal domains was again affirmed by this contest.

The contest also highlighted the need to improve university educational processes for IC design to better equip students to design fully functional mixed-signal chips containing hundreds of millions of transistors so that they function correctly on the first silicon pass. Teams had testing and verification strategies but none were comprehensive enough to find and overcome all critical design errors. "The SRC design contest has been a wonderful learning opportunity for our team. We believe that by going through the implementation and testing phases of the project we have grown as engineers and researchers," said student Mark Hempstead of the Harvard team.

The University of Virginia team, led by Professor Mircea Stan, took second place with their entry, "An SRAD Image Processor as a Reconfigurable, Temperature-Aware SoC Designed for Low-Power Operation." This is a design of a low-power ultrasound system-on-chip for portable image processing applications, using an efficient algorithm to increase signal-to-noise performance.

The team from Michigan State University, led by Professor Peixin Zhong, came in third in the competition with their entry, "Adaptive Sensor Network Platform Chip." This design creates a platform with flexible sensor interface suitable for scanning an array of inputs of different types for a broad range of applications.

The SRC/SIA SoC Design Challenge was sponsored by major companies and organizations of the semiconductor industry, including SRC, SIA, Advanced Micro Devices, AMI Semiconductor, Analog Devices, Cadence Design Systems, Freescale Semiconductor, IBM, Intel, MOSIS, National Semiconductor and Texas Instruments, contributing more than \$300,000 to host this contest that began in January 2005. The awards included a total of \$65,000 in cash for phases one and two, plus \$250,000 in fabrication services.

About SRC

As the pioneer of collaborative research for the semiconductor industry, SRC defines industry needs, invests in and manages the research that gives its members a competitive advantage in the dynamic global marketplace. SRC expands the industry knowledge base and attracts premier students to help innovate and transfer semiconductor technology to the commercial industry. Established in 1982, SRC is based in Research Triangle Park, N.C., and drives long-term semiconductor research contracts on behalf of its participating members: Advanced Micro Devices, Inc., Applied Materials, Inc., Axcelis Technologies, Inc., Cadence Design Systems, Freescale Semiconductor, Inc., Hewlett-Packard Co., IBM Corp., Intel Corp., LSI Logic Corp., Mentor Graphics Corp., The Mitre Corp., Novellus Systems, Inc., Rohm and Haas Electronic Materials and Texas Instruments Corp.

SRC also seeks to leverage funding from global government agencies. For more information, visit www.src.org.

About SIA

The SIA is the leading voice for the semiconductor industry and has represented U.S. semiconductor companies since 1977 and SIA member companies comprise more than 85% of the U.S. semiconductor industry. Collectively, the chip industry employs a domestic workforce of 225,000 people. More information about the SIA can be found at www.sia-online.org.

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