Mark D. Hempstead

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(Updated Dec 30th 2014)

EDUCATION

PhD, Engineering Sciences, June 2009,
Harvard University, Cambridge MA
Academic Advisors: Prof. Gu-Yeon Wei and Prof. David Brooks (Co-Advised)
*Dissertation: "*Accelerator-Based Architectures for Wireless Sensor Network Applications"
Dissertation Committee: Prof. Gu-Yeon Wei, Prof. David Brooks, Prof. Margo Seltzer

S.M Engineering Sciences, June 2005
Harvard University, Cambridge MA

B.S. Computer Engineering, Summa Cum Laude, May 2003
Tufts University, Medford MA

HONORS, AWARDS AND MEMBERSHIPS

2014 Drexel University Allen Rothwarf Award for Teaching Excellence
2014 Drexel College of Engineering Excellence in Research Award
2014 NSF CAREER Award
2012 HPCA Best Paper Nominee
2006 SRC Design Contest Winner
2002- Member Eta Kappa Nu Electrical Engineering Honor Society
2002- Member Tau Beta Pi Engineering Honor Society

Memberships: IEEE, ACM, IEEE Computer Society, ACM SIGARCH

WORK EXPERIENCE

Drexel University, Philadelphia PA **Junior Colehower Chair Assistant Professor** **1/2010 – present**
Developed a research program in power-aware computer architecture, low power circuit design, and power-aware systems. Current research topics include energy-efficient microarchitecture, accelerator-based architectures, workload characterization, and power-agile computing. Re-imagined the both the undergraduate and graduate computer architecture sequences to include multi-core processing and power-aware. Winner of University wide teaching award and NSF CAREER award. Advisor to ten graduate students: 8 PhD and 2 MS.

ARM Ltd., Cambridge UK **Research Intern, PostDoc, R&D** **7/2009 – 11/2009**
Developing a system level power modeling infrastructure for SoC

Harvard University, Cambridge MA **Research Assistant** **9/2003 – 6/2009**

Modeling of multi-core vs. accelerator-based architectures in the context of future technologies. Investigated low power architecture and circuit techniques for wireless sensor network applications under Prof. Gu-Yeon Wei and Prof. David Brooks. Evaluated architecture and circuit ideas and taped out microprocessor prototypes in 130 nm and 180 nm CMOS and tested the results.

Intel Corporation, Hudson MA **Research Intern, VSSAD Group 5/2005 – 8/2005**
Conducted a study of the performance and power tradeoffs of x86 decoding structures. Modified a P6 based simulator and ran extensive simulations of real traces. Prepared a final report for use in future internal projects.

TEACHING EXPERIENCE

At Drexel as Course Designer and Course Lead:

ECEC-414	High Performance Computing (UG)	Winter 2014, Spring 2012
ECEC-412	Modern Processor Design (UG)	Winter'15, Fall'13, Spring'13, W'12
ECEC-623	Adv. Parallel Computer Architecture (Grad)	Spring 2014, Winter 2013, Spring'11
ECEC-622	Parallel Computer Architecture (Grad)	Winter 2011, Spring 2010
ECEC-621	High Performance Computer Architecture (Grad)	Winter'15, W'14, F'12, F'10, W '10
ECEC-690	Advanced Programming Graduate Students	Fall 2014

At Drexel as Recitation Instructor:

ENGR-232	Dynamic Engineering Systems	Winter 2012
ECE-200	Digital Logic Design	Spring'14, Fall '13, Spring '12, Fall'11

Tufts University **Lecturer**

EE26	Digital logic systems	Spring 2009

Resident Tutor, Lowell House Harvard University – (9/2006 – 6/2009) Living in a undergraduate residence. Responsible for the resident life of 35 undergraduates. Responsibilities also include academic advising.

ARCHIVAL PEER-REVIEWED JOURNAL, CONFERENCE PUBLICATIONS

SynchroTrace: Synchronization-aware Architecture-agnostic Traces for Light-Weight Multicore Simulation. Siddharth Nilakantan, Karthik Sangaiah, Ankit More, Giordano Salvador, Baris Taskin, Mark Hempstead, *To Appear in IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), March. 2015.*

Effects of Non-determinism in Hardware and Software Simulation with Thread Mapping. Giordano Salvador, Siddharth Nilakantan, Ankit More, Baris Taskin, M. Hempstead*, 28th International Conference on VLSI Design and 14th International Conference on Embedded System Design 2015 (VLSID ES),* Jan. 2015.

Can you trust your memory trace?: A comparison of memory traces from binary instrumentation and simulation. Siddharth Nilakantan, Scott Lerner, M. Hempstead, Baris Taskin. *28th International Conference on VLSI Design and 14th International Conference on Embedded System Design 2015 (VLSID ES)*, Jan. 2015.

Static Thread Mapping for NoC CMPs via Binary Instrumentation Traces. Giordano Salvador, Siddharth Nilakantan, Ankit More, Baris Taskin, M. Hempstead. *32nd IEEE International Conference on Computer Design 2014 (ICCD), Oct. 2014.*

Epoch Profiles: Microarchitecture-Independent Application Analysis and Microarchitectural Optimization. Trevor E. Carlson, Siddharth Nilakantan, M. Hempstead, Wim Heirman. *IEEE Computer Architecture Letters (CAL), Jan-July 2014.*

Register Allocation and VDD-gating algorithms for Out-of-Order Architectures. Steven Battle, and Mark Hempstead. *International Conference on Computer Design (ICCD). Oct 2013.* **(acceptance rate: 25%)**

Characterizing the Costs and Benefits of Hardware Parallellism in Accelerator Cores. Steven Battle, and Mark Hempstead. *International Conference on Computer Design (ICCD). Oct 2013.* **(acceptance rate: 25%)**

Platform-independent characterization of function-level communication in workloads using Dynamic Binary Instrumentation. Siddharth Nilakantan, Mark Hempstead. *In 2013 IEEE International Symposium on Workload Characterization (IISWC). Sept 2013.* **(acceptance rate: 30%)**

Metrics for Early-Stage Modeling of Many-Accelerator Architectures. Siddharth Nilakantan, Steven Battle, and Mark Hempstead. *Computer Architecture Letters (CAL), 2012.* ***(acceptance rate: 24%)***

Flexible Register Management using Reference Counting. Steven Battle, Andrew Hilton, Mark Hempstead, Amir Roth. *International Symposium on High Performance Computer Architecture (HPCA) . Feb 2012* ***(acceptance rate: 17%, citations: 2) [Best Paper Nominee]***

The Accelerator Store Framework for High-Performance, Low-Power Accelerator-based Systems Mike Lyons, Mark Hempstead, David Brooks, Gu-Yeon Wei. *ACM Transactions on Architecture and Code Optimization (TACO). Also Invited Presentation at HiPEAC, Paris France. January, 2012.* ***(citations: 6)***

Evaluation of an Accelerator Architecture for Speckle Reducing Anisotropic Diffusion. Siddharth Nilakantan, Srikanth Annangi, Nikhil Gulati, Karthik Sangaiah and Mark Hempstead. *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES). Taipei, Taiwan, October 2011.* ***(acceptance rate: 38%, citations 2)***

An Accelerator-Based Wireless Sensor Network Processor in 130 nm CMOS. Mark Hempstead, Gu-Yeon Wei, and David Brooks. *IEEE Transactions on Emerging and Selected Topics in Circuits and Systems (JETCAS). Vol. 1, Num 2. June 2011****(citations: 19)***

The Case for Power-Agile Computing, Geoffrey Challen, Mark Hempstead. *USENIX Workshop on Hot Topics in Operating Systems (HotOS), May 2011.* ***(acceptance rate: 25%, citations: 3)***

The Accelerator Store framework for high-performance, low-power accelerator-based systems. Michael Lyons, Mark Hempstead, Gu-Yeon Wei, and David Brooks. *Computer Architecture Letters (CAL) Nov 2010.* ***(acceptance rate: 24%, citations: 10)***

Architecture and Circuit Techniques for Low-Throughput, Energy-Constrained Systems Across Technology Generations, Mark Hempstead, Gu-Yeon Wei and David Brooks. *In Proceedings of the International Conference On Compilers, Architecture, And Synthesis For Embedded Systems (CASES).* Seoul South Korea. October 2006.**(aceeptance rate: 41%, citations: 19)**

A Realistic Power Consumption Model for Wireless Sensor Network Devices, Qin Wang, Mark Hempstead, and Woodward Yang. *In Proceedings of the Third Annual IEEE Communications Society Conference on Sensor, Mesh and Ad Hoc Communications and Networks (SECON). Reston, VA, September 2006.* ***(acceptance rate: 26%, citations: 202)***

Power and Thermal Effects of SRAM vs. Latch-Mux Design Styles and Clock Gating Choices. Yingmin Li, Mark Hempstead, Patrick Mauro, David Brooks, Zhigang Hu, Kevin Skadron. *In Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED'05),* San Diego, CA, August 2005 ***(acceptance rate: 23%, citations: 6)***

An Ultra Low Power System Architecture for Wireless Sensor Network Applications, Mark Hempstead, Nikhil Tripathi, Patrick Mauro, Gu-Yeon Wei, and David Brooks *In Proceedings of the 32nd International Symposium on Computer Architecture (ISCA)*, Madison, WI, June 2005. ***(acceptance rate: 23%, citations: 141)***

Simulating the Power Consumption of Large-Scale Sensor Network Applications, Victor Shnayder, Mark Hempstead, Bor-rong Chen, Geoff Werner-Allen, and Matt Welsh. *In Proceedings of the Second ACM Conference on Embedded Networked Sensor Systems (SenSys'04)*, Baltimore, MD, November 2004 ***(acceptance rate: 14%, citations: 943)***

INVITED AND WORKSHOP PUBLICATIONS

"Prioritizing Energy Usage by Allocating Inefficiency," Guru Prasad Srinivasa, Rizwana Begum, M. Hempstead, Geoffrey Challen**,** *Appears in International Workshop on Mobile Computing Systems and Applications (HotMobile),* Feb 2014.

Vertical Arbitration-free 3D NoCs. A. More, S. Nilakantan, M. Hempstead, B. Taskin. *Proc. Work-In-Progress (WiP) at ACM/IEEE Design Automation Conference (DAC),* June 2013

An Accelerator-based Wireless Sensor Network Processor in 130nm CMOS," Invited paper. Mark Hempstead, Gu-Yeon Wei, and David Brooks. International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES-09), Grenoble, France, Oct. 2009.

Navigo: An early-stage model to study power-constrained architectures and specialization Mark Hempstead, Gu-Yeon Wei and David Brooks**.** ISCA Workshop on Modeling, Benchmarking, and Simulations (MoBS), June 2009. ***(citations: 23)***

An accelerator-based wireless sensor network processor in 130nm CMOS Mark Hempstead, Gu-Yeon Wei and David Brooks ISCA Workshop on Architectural Research Prototyping (WARP), June 2009.

System Design Considerations for Sensor Network Applications (Invited) Mark Hempstead, Gu-Yeon Wei, and David Brooks. *International Symposium on Circuits and Systems (ISCAS).* Seattle WA., May 2008. (Invited Session: Energy-Efficient Building Blocks for Ubiquitous Sensing)

Survey of hardware systems for wireless sensor networks (Invited) Mark Hempstead, Michael J. Lyons, David Brooks and Gu-Yeon Wei. *ASP Journal of Low Power Electronics*, Vol. 4., No. 1, April 2008. ***(citations: 44)***

Ultra Low Power System Architecture for Wireless Sensor Network Applications Mark Hempstead, Gu-Yeon Wei, and David Brooks. *Nanoelectronic Devices for Defense & Security Conference (NANO-DDS).* Washington D.C., June 2007.

Design and Implementation of An Ultra Low Power System Architecture for Wireless Sensor Network Applications (Design Contest), Mark Hempstead, Xiaoyao Liang, Patrick Mauro, Gu-Yeon Wei, and David Brooks *SRC Student Symposium – SoC design contest Phase 2, 1st place.* Raleigh/Durham NC, October 2006.

Design and Implementation of An Ultra Low Power System Architecture for Wireless Sensor Network Applications (Design Contest), Mark Hempstead, Xiaoyao Liang, Patrick Mauro, Gu-Yeon Wei, and David Brooks *SRC Techcon – SoC design contest Phase 1, 2nd place*. Portland, OR, October 2005.

TinyBench: The Case For A Standardized Benchmark Suite for TinyOS Based Wireless Sensor Network Devices, Mark Hempstead, David Brooks, and Matt Welsh. *In Proceedings of the First IEEE Workshop on Embedded Networked Sensors (EmNets'04),* Tampa FL November 2004. ***(citations: 27)***

RESEARCH FUNDING

"Fast and Efficient Hardware Design Exploration through Memory-NoC Analysis for Multi-Core SoCs" 10/1/2014 – 9/30/2015. **$100,00.** Samsung GRO program: Next Generation Computing Ultra Low-Power Computing For Wearable IoT Devices.

"CSR: Medium: Collaborative Research: Architecture and System Support for Power-Agile Computing." 8/1/2014 – 7/31/2016. **$278,836** (Drexel Portion). National Science Foundation (NSF)

"CAREER: Combating Dark Silicon through Specialization: Communication-Aware Tiled Many-Accelerator Architectures" 2/1/2014 – 1/31/2019. **$470,000**. National Science Foundation (NSF)

"II-NEW: Testbed for High Performance Interconnects" Co-PI (PI is Baris Taskin) 10/1/2013 – 09/31/2016. **$700,000.** National Science Foundation (NSF)

"AfterBurner: Efficient Performance Scaling via Post-Retirement Processing" Subcontract. (PI is Milo Martin) 1/1/2013 – 8/31/2014. **$182,996**. University of Pennsylvania and National Science Foundation (NSF).

"Performance Estimation and Optimization of REDHAWK SDR Applications" PI. (Co-PIs Moshe Kam, Kapil Dandekar, and Jeremy Johnson) 1/1/2013 – 6/30/3015. Amount and Sponsor Confidential.

"SHF: Small: AfterBurner: Efficient Performance Scaling via Post-Retirement Processing" Co-PI (PI is Amir Roth at UPenn) 9/1/2010 – 12/31/2011. **$118,999** National Science Foundation (NSF).

PRESENTATIONS AND TALKS

10/2013	Keynote at ICCD Conference. "Combating Dark Silicon: It Takes a Village". Ashville NC.
4/2012	ISPASS FastPath Workshop Invited Speaker "Ultra-Low Power Computing with Accelerator-based Architectures"
10/2011	"Ultra-Low Power Computing with Accelerator-based Architectures", Drexel University CS Dept
4/2011	"From Sensor Networks to Accelerator-based Architectures" NCSU
11/2010	"Designing Ultra Low-Power Systems for Wireless Sensor Networks", Swarthmore College
9/2010	"Designing Ultra Low-Power Systems for Wireless Sensor Networks", Princeton University

4/2010	"Designing Ultra Low-Power Systems for Wireless Sensor Networks", Washington University, St. Louis
7/2009	"Designing Ultra Low-Power Systems for Wireless Sensor Networks", ARM Ltd., Cambridge United Kingdom
6/2009	MOBS at ISCA, Austin Texas – "Navigo: An early-stage model to study power-constrained architectures and specialization"
6/2009	WARP at ISCA, Austin Texas – "An accelerator-based wireless sensor network processor in 130nm CMOS"
6/2009	"Designing Ultra Low-Power Systems for Wireless Sensor Networks", University of Massachusetts Dartmouth
4/2009	"Designing Ultra Low-Power Systems for Wireless Sensor Networks", Columbia University
3/2009	"Designing Ultra Low-Power Systems for Wireless Sensor Networks", Bucknell University
1/2009	"Designing Ultra Low-Power Systems for Wireless Sensor Networks", Drexel University
10/2008	"Designing Ultra Low-Power Systems for Wireless Sensor Networks", Tufts University
5/2008	ISCAS Seattle WA – "System Design Considerations for Sensor Network Applications"
6/2007	NANO-DDS, Washington DC – "Ultra Low Power System Architecture for Wireless Sensor Network Applications"
10/2006	SRC Student Symposium, Raleigh/Durham NC – "Design and Implementation of An Ultra Low Power System Architecture for Wireless Sensor Network Applications"
10/2006	CASES, Seoul South Korea – "Architecture and Circuit Techniques for Low-Throughput, Energy-Constrained Systems Across Technology Generations"
10/2005	SRC Techcon, Portland OR – "Design and Implementation of An Ultra Low Power System Architecture for Wireless Sensor Network Applications"
6/2005	ISCA, Madison WI – "An Ultra Low Power System Architecture for Wireless Sensor Network Applications"

CURRENT GRADUATE STUDENTS

Steven Battle, Ph.D. Candidate, successful defense August, 2014. Graduation fall 2014.
Siddharth Nilakantan, Ph.D. Candidate, Expected to graduate in March, 2015.
Rizwana Begum, Ph.D Candidate
Jonathan Stokes, PhD Student
Karthik Sangaiah, PhD Student (Co-advised), NSF GREP Fellowship Winner
Cesar Gomes, PhD Student, GEM Fellowship Winner
Parnian Mokri, PhD Student
David Werner, post-BS PhD Student

GRADUATED STUDENTS

Jason Palaszewski, M.S.
Tianyun Zhang, M.S.

UNIVERSITY SERVICE

2014	Department Chair Search Committee, Electrical and Computer Engineering
2014-2013	Distinguished Lecture Series in Computer Engineering Organizer
2013-2011	Computer Engineering Faculty Search Committee
2014-2011	ECE Senior Design Committee
2012	Computer Science Faculty Search Committee
2014-2012	Member of Academic Council and volunteer instructor for Drexel University Computing Academy (DUCA), a five week residential summer program for high school students.
2010	ECE Department Development Committee

PROFESSIONAL SERVICE AND REVIEWING ACTIVITY

Conference Organization:

1. External Review Committee, IEEE International Symposium on Computer Architecture (ISCA), 2105
2. Registration Chair, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2015
3. External Review Committee, IEEE International Symposium on High Performance Computer Architecture (HPCA), 2015
4. Program Committee, International Conference on Compilers, Architectures and Synthesis of Embedded Systems (CASES) 2014
5. Publications Chair, IEEE International Symposium on Workload Characterization (IISWC) 2014
6. Publications Chair, International Symposium on Performance Analysis of Systems and Software (ISPASS) 2014
7. Program Committee, IEEE International Symposium on Workload Characterization (IISWC) 2013
8. Publications Chair, International Symposium on Performance Analysis of Systems and Software (ISPASS) 2013
9. Workshop Organizer, Accelerator Architectures for General-Purpose Computing: from a Hardware, System Software and Application Perspective with HPCA 2012
10. Publications Chair, International Symposium on Performance Analysis of Systems and Software (ISPASS) 2012
11. Program Committee, Workshop Computer Architecture and Operating System Co-design (CAOS) 2012
12. Publications Chair, International Symposium on Performance Analysis of Systems and Software (ISPASS) 2011

Grant Proposal Panel Reviewer:

1. 2014 One NSF Panel
2. 2013 One NSF Panel

Reviewer (Since 2010):

1. 2010 ACM Transactions on Sensor Networks
2. 2010 IEEE Transactions on CAD
3. 2010 IEEE Transactions on Computers (ToC)

4. 2010 IEEE Transactions on Wireless Communications
5. 2010 ACM Transactions on Architecture and Code Optimization (TACO)
6. 2011 IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)
7. 2011 The International Journal of Computer and Telecommunications Networking (COMNET)
8. 2011 International Symposium on High Performance Computer Architecture (HPCA)
9. 2011 IEEE Transactions on Computers
10. 2011 HPCA Workshop on Architectural Reliability (WRA)
11. 2012 International Symposium on High Performance Computer Architecture (HPCA)
12. 2012 ACM Transactions on Architecture and Code Optimization (TACO)
13. 2012 IEEE Transactions on Computers (ToC)
14. 2013 Computer Architecture Letters (CAL)
15. 2013 IEEE Micro
16. 2013 ACM Transactions on Architecture and Code Optimization (TACO)
17. 2013 IEEE Transactions on Computers (ToC)
18. 2013 IEEE International Symposium on Workload Characterization (IISWC)
19. 2014 ACM Transactions on Architecture and Code Optimization (TACO)
20. 2014 Computer Architecture Letters (CAL)